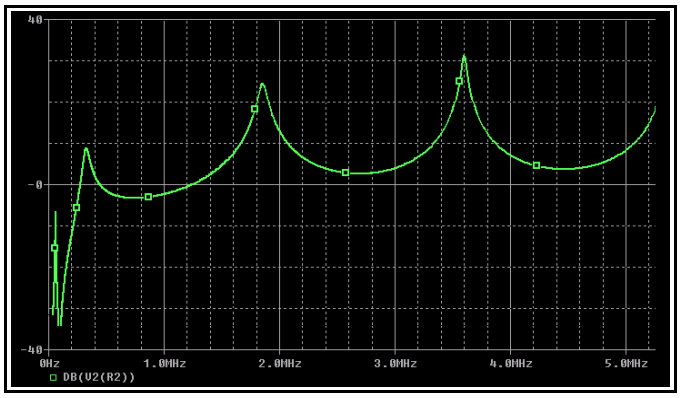
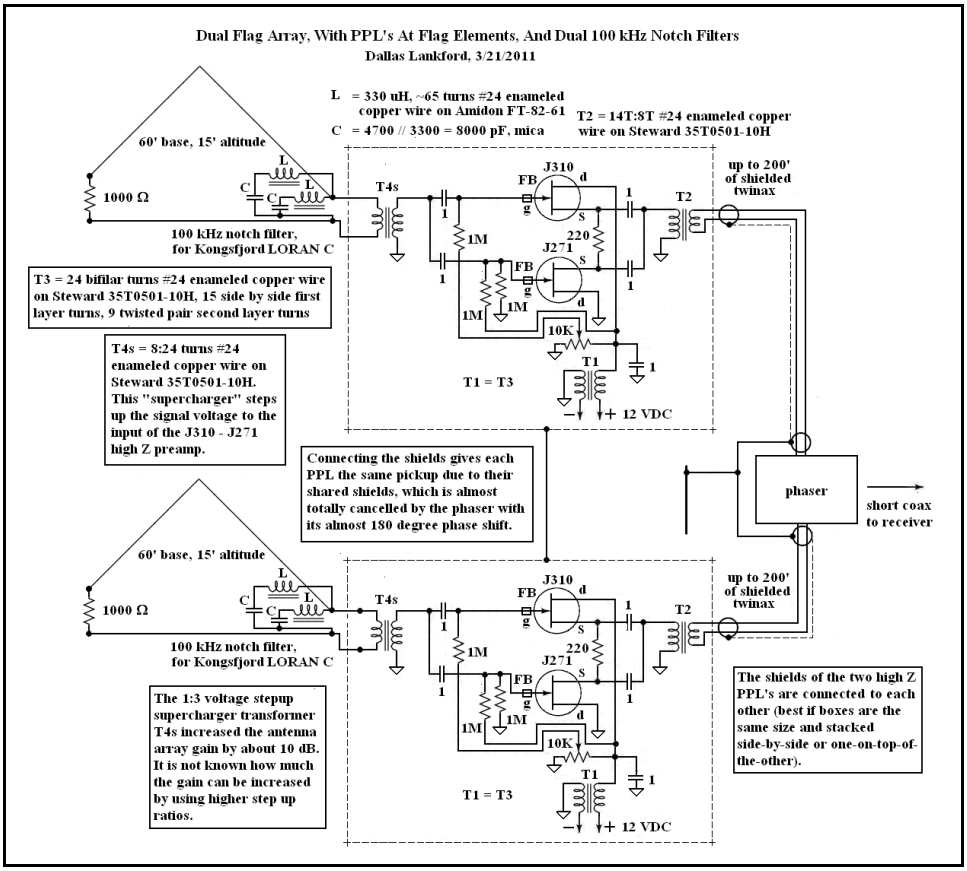
Dual And Quad MW PPL Flag Arrays

Dallas Lankford, 3/24/2011

Capacitor terminated loop arrays with PPL's at the receiver end of 200' of twinax were developed because they gave more gain increase than flag arrays, and because they simplified construction of quad arrays by putting the PPL's in the phaser box. Unfortunately, it was recently discovered that the maximum null depth of the pattern of dual capacitor terminated loop arrays in the neighborhood of the resonant frequency (within 15% or so of the resonant frequency) was degraded by 10 dB or more unless the terminating capacitors were carefully adjusted as described in "Waller Loop Arrays." It is presently unknown how to recover such null loss for quad arrays. Another undesirable (but apparently curable) feature of capacitor terminated arrays with PPL's at the receiver end of 200' of shielded twinax was multiple resonances throughout the SW bands which were revealed by PSpice simulations like the one at right. They may also have been observed during early testing of the dual capacitor terminated loop arrays because the Perseus ADC clipping red light came on regularly at night until a 2 MHz 5 element Chebyshev low pass filter was added at the antenna input of Perseus. The cause of the ADC clipping was likely European broadcast signals in the 60 and 31 meter bands enhanced by two of the resonances.

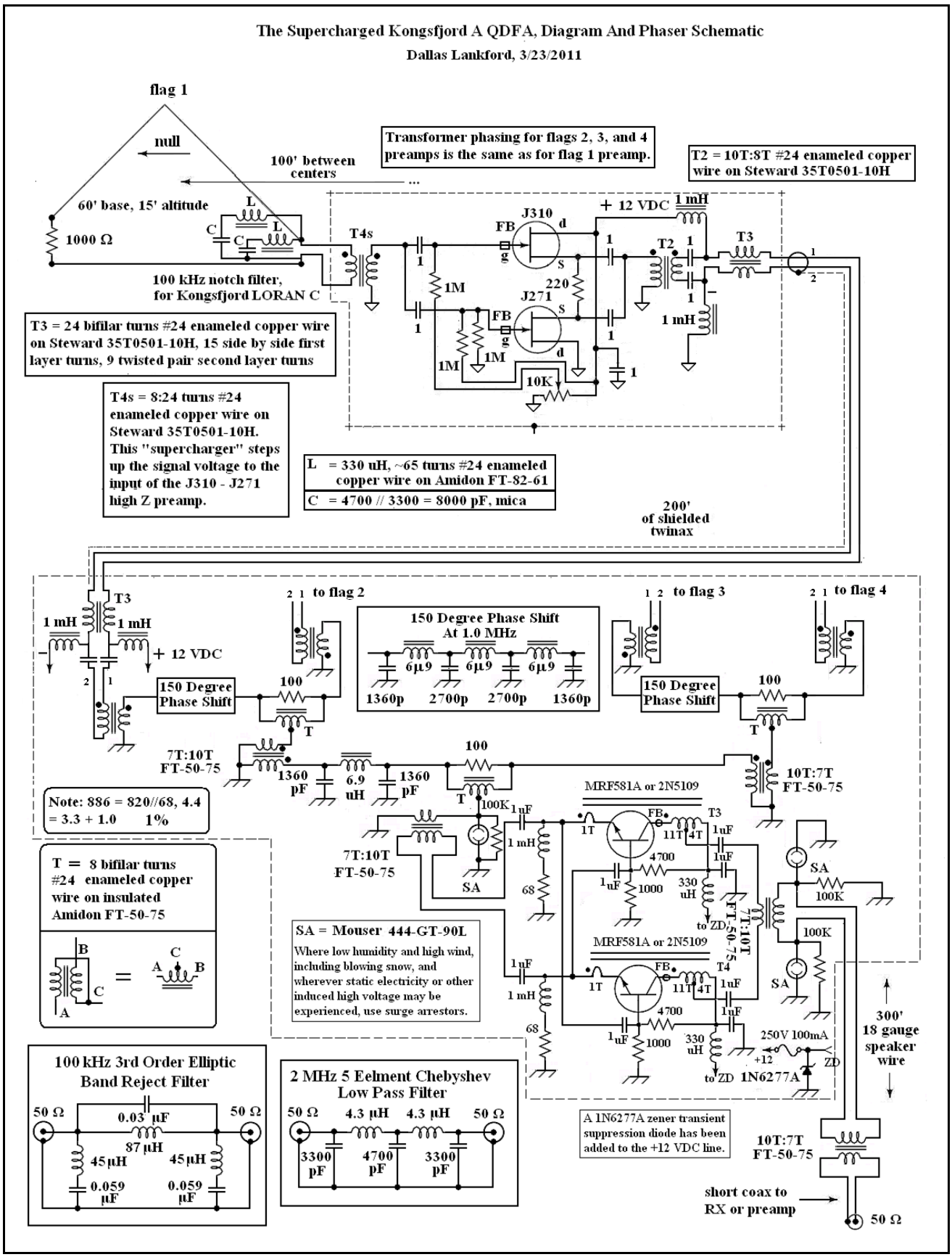


Dual and quad pure flag arrays have no capacitors, and so no null reduction. PPL's alone at the flag elements increase the low MW band gain of a standard dual flag array by 13 dB, and the "superchargers" (1:3 turns ratio step up transformers at the inputs to the PPL's) increase the gain by another 5 dB, a total of 18 dB increase, cf. High Z PPL's + Loop And Flag Arrays . When dual and quad flag array PPL's are placed at the receiver ends of the lead ins, the gain increases due to the PPL's are as much as 8 to 10 dB less than when the PPL's are at the flag elements. Also, with PPL's at the flag elements the multiple resonances are eliminated. For these reasons dual and quad flag arrays should place the PPL's at the flag antenna elements.



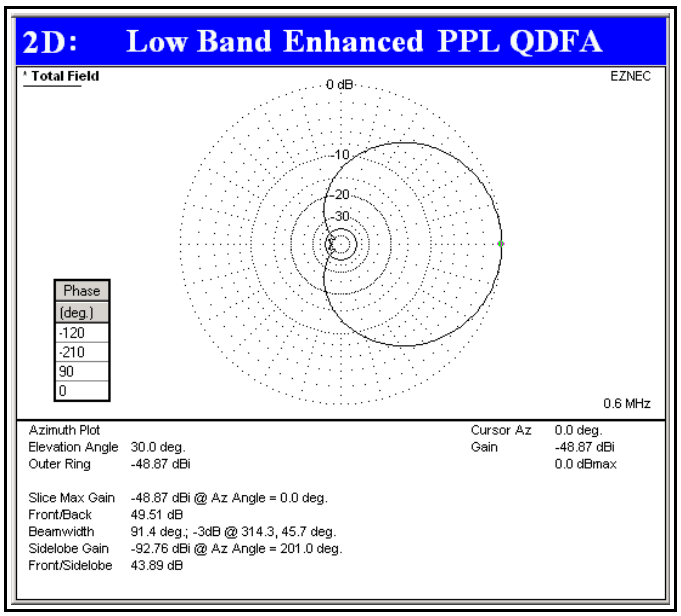
Above right is a schematic of a dual flag array with PPL's at the flag elements. Common mode chokes are not shown, but they should be used in the lead ins signal paths.

Below is a schematic of a quad flag array with PPL's at the flag elements, including common mode chokes in the signal paths.


The Supercharged Kongsfjord A QDFA, Diagram And Phaser Schematic
Dallas Lankford, 3/23/2011
flag 1
null
100' between centers
60' base, 15' altitude
1000 Ω
100 kHz notch filter, for Kongsfjord LORAN C
Transformer phasing for flags 2, 3, and 4 preamps is the same as for flag 1 preamp.
T2 = 10T:8T #24 enameled copper wire on Steward 35T0501-10H
+ 12 VDC
1 mH
J310
J271
FB
T4s
T2
T3
1M
220
10K
T3 = 24 bifilar turns #24 enameled copper wire on Steward 35T0501-10H, 15 side by side first layer turns, 9 twisted pair second layer turns
T4s = 8:24 turns #24 enameled copper wire on Steward 35T0501-10H. This "supercharger" steps up the signal voltage to the input of the J310 - J271 high Z preamp.
L = 330 uH, ~65 turns #24 enameled copper wire on Amidon FT-82-61
C = 4700 // 3300 = 8000 pF, mica
200' of shielded twinax
to flag 2
to flag 3
to flag 4
150 Degree Phase Shift
150 Degree Phase Shift At 1.0 MHz
6µ9
1360p
2700p
100
7T:10T FT-50-75
1360 pF
6.9 uH
10T:7T FT-50-75
MRF581A or 2N5109
100K
1uF
1 mH
68
4700
1000
330 uH
11T
4T
SA
SA = Mouser 444-GT-90L
Where low humidity and high wind, including blowing snow, and wherever static electricity or other induced high voltage may be experienced, use surge arrestors.
Note: 886 = 820//68, 4.4 = 3.3 + 1.0 1%
T = 8 bifilar turns #24 enameled copper wire on insulated Amidon FT-50-75
A
B
C
to ZD
ZD
1N6277A
250V 100mA
+12
A 1N6277A zener transient suppression diode has been added to the +12 VDC line.
300' 18 gauge speaker wire
short coax to RX or preamp
50 Ω
100 kHz 3rd Order Elliptic Band Reject Filter
0.03 µF
87 µH
45µH
0.059 µF
2 MHz 5 Eelment Chebyshev Low Pass Filter
4.3 µH
3300 pF
4700 pF

The QDFA with PPL's at flag elements is designed to get DC power from the phaser box through the twinax. Battery power of the PPL's is an option if noise enters the PPL's via the DC power feeds.

The 18 dB gain increase compared to a standard QDFA is excellent, but I wanted more low band gain increase, as I had gotten with the capacitor terminated QDFA. But I wanted the low band gain increase without using capacitors which degraded the null. After many EZNEC simulations I arrived at the pattern at right with about 10 dB low band gain increase (and only 2.5 dB high band gain increase which levels the array gain). The null aperture is slightly narrower than the original QDFA, but so slight that it will have little or no effect on splatter reduction. The new phases of the low band enhanced QDFA phaser are included in the schematic above.



The dual PPL array with PPL's at the flag elements and 100 kHz notch filters has been tested extensively. These tests were necessary for there to be a high probability that the low band enhanced PPL QDFA will perform as designed. It is believed that modifications of the dual PPL array design above (without the 100 kHz notch filters if LORAN C is not an issue) will improve the performance of the WF, HWF, and GWF arrays developed by NX4D and N4IS upon which this work was inspired.